A Four-Legged Loop Inverter for Two-Lane Dynamic Wireless Power Transfer

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***Abstract*—Two-lane wireless power transfer has been proposed to reduce EMI in semi-DWPT effectively. A novel inverter topology called a four-legged loop inverter (4LL) is proposed for such configurations. The 4LL can activate two pairs of coils independently without selection switches, and the number of MOSFETs (metal oxide semiconductor field-effect transistor) is halved compared to the H-bridge. Both PWM (pulse width modulation) and PDM (pulse density modulation) control are possible. Phase control is proposed to keep current from flowing in inactive coils under uneven load conditions. The results are verified in simulations and experiments.**

***Index Terms*—Dynamic Wireless Power Transfer, 4-legged Loop Inverter, Phase Adjustment Control**

Introduction

Semi-DWPT (Dynamic Wireless Power Transfer [1]) in urban settings allows for reduced battery capacity in EVs (Electric Vehicles). As shown in Fig. 1, 2-lane DWPT [2] has been proposed for horizontal cancellation of EMI (Electromagnetic Interference [3], [4]) by activating the left-side and right-side coils simultaneously in opposite current phase.

H-bridge inverters are commonly used as shown in Fig. 2(a) but the cost of implementation is a concern [5]. Various inverter topologies for activating multiple Tx coils with fewer MOSFETs have been proposed, including parallel connection of coils [6] and n-legged inverters [7]. However, in the case of 2-lane DWPT, it is possible to implement a topology that can halve the number of MOSFETs compared to the H-bridge without using selection switches for each coil.

This paper is organized as follows. Section introduces the 4-legged loop (4LL) Inverter and describes its operation under ideal conditions, with simulation results. In section , phase adjustment control is proposed to prevent the false activation of inactive coils under uneven load conditions. In section -A, the experiment conditions and results are discussed, and the proposed 4LL inverter is shown to be effective. Section -A concludes the paper.

4-Legged Loop Inverter

Basic operation

The 4LL Inverter is shown in Fig. 2(b). Q1-Q8 are the MOSFETs, V_{DC} and V_{Batt} are the DC voltage and the battery voltage, V_1-V_4 are the output voltages of legs 1-4, V_{X} and I_{X} (X=L1, R1, L2, R2, Lr, Rr) are the input/output AC voltage and current for the corresponding loads, R_{X}, L_{X}, and C_{X} (X=L1, R1, L2, R2, Lr, Rr) are the resistance, inductance, and capacitance of each load, and M_{L} and M_{R} are the mutual inductances for the left lane and the right lane, in this case between L_{L1} and L_{Lr} for M_{L} and L_{R1} and L_{Rr} for M_{R}. The physical placement of each load (L1, R1, L2, R2, Lr, Rr) on a road is shown in Fig. 1.

Under ideal 4LL operation, loads L1 and R1 would be activated with the current in opposite phases while L2 and R2 are inactive, and vice versa. The gate signals for such operation are shown in Fig. 3. Fig. 3(a) shows the gate signals for activating loads L1 and R1, while Fig. 3(b) is for L2 and R2. In Fig. 3(a), the gate signals of leg 1(Q1 and Q2) are identical to those of leg 4 (Q7 and Q8), and those of leg 2 (Q3 and Q4) are identical to those of leg 3 (Q5 and Q6). Under ideal conditions, this ensures that loads L2 and R2 remain inactive, as $V_1 = V_4$ and $V_2 = V_3$, and therefore $V_{\mathrm{L2}} = 0$ and

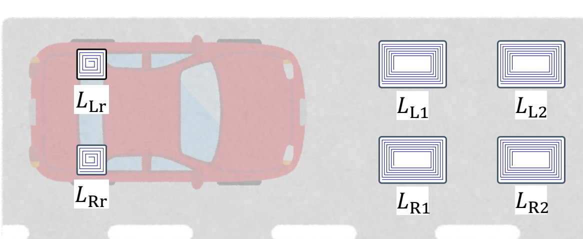

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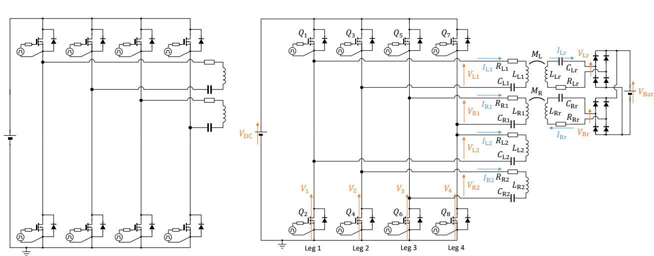
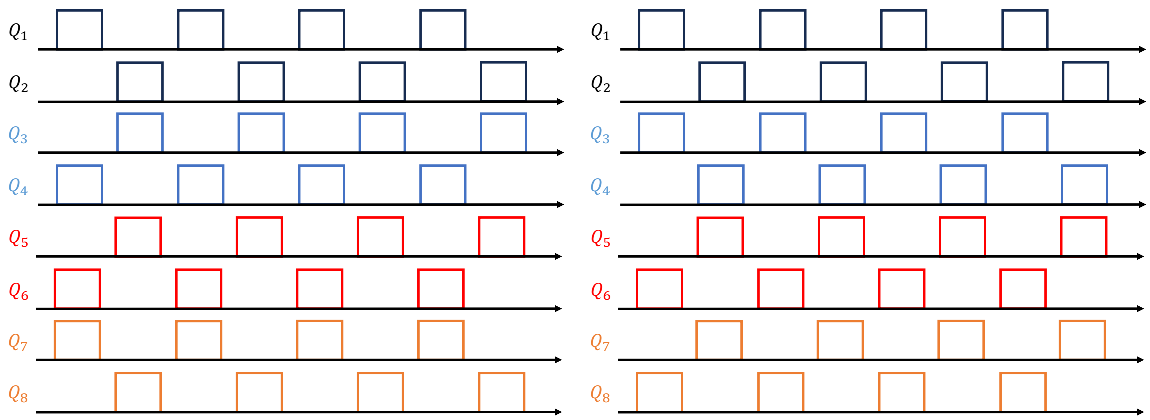
Fig. 1. 2 lane DWPT configuration



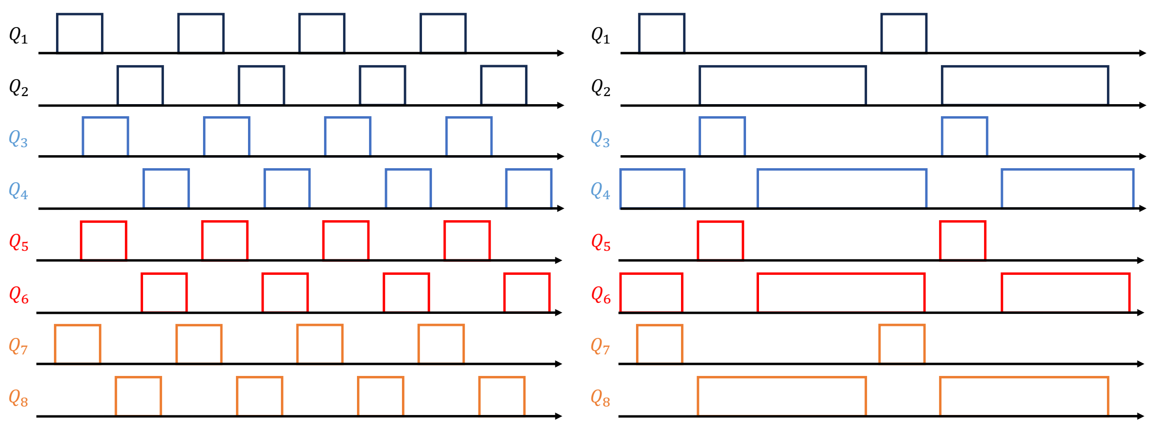
(a) H-bridge inverter (b) 4-legged Loop inverter

Fig. 2. H-bridge and 4-legged loop inverter topologies.



(a) Loads L1 and R1 activation (b) Loads L2 and R2 activation

Fig. 3. Gate signal for activation of (a) L1, R1 and (b) L2, R2



(a) PWM control (b) PDM control

Fig. 4. (a) PWM and (b) PDM control for the 4LL

$V_{\mathrm{R2}} = 0$. The opposite is true for Fig. 3(b), with $V_1 = V_2$ and $V_3 = V_4$, and therefore $V_{\mathrm{L1}} = 0$ and $V_{\mathrm{R1}} = 0$.

As long as the abovementioned relationship holds true, the inactive load pairs will remain inactivated. Therefore, for Fig. 3(a), the phase difference between the gate signals of legs 1 and 2 and legs 3 and 4 can each be modulated for PWM control as shown in Fig. 4(a) and the pulse density can be modulated as shown in Fig. 4(b).

Simulation Verification

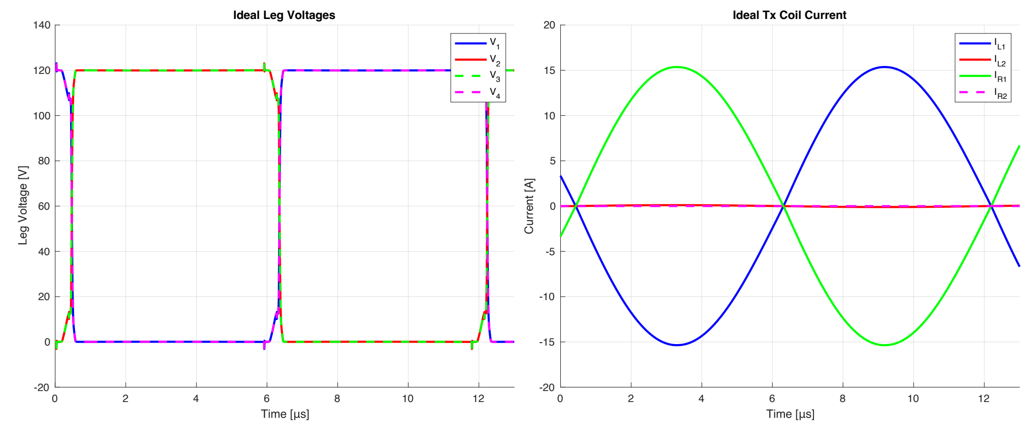
Simulink was used to simulate the behavior of 4LL under ideal conditions, with the parameter for each Tx load identical to that of load L1 and Rx load identical to load Lr, in table I. L_{L1} and L_{R1} are coupled to the Rx coils. The waveforms for leg output voltages V_1-V_4 and Tx currents I_{X} (X=L1, R1, L2, R2) are shown in Fig. 5. Leg output voltage pairs V_4, V_1 and V_2, V_3 are each identical to each other, and opposite in phase to the other pair. Therefore, I_{L1} and I_{R1} are active while I_{L2} and I_{R2} are nearly zero.

Phase Adjustment Control

Under actual conditions, the parameters for the left and right loads are not always identical. Self-inductance variations and coupling variations are especially likely to occur in DWPT conditions, resulting in variations between I_{L1} and I_{R1}, for example. In such cases, voltage difference is applied to the inactive loads due to the different deadtime voltage waveforms [8]. This causes the false activation of inactive coils.

Phase adjustment control is proposed to prevent false activation. In the ideal gate signals shown in Fig. 3(a), the identical gate signals of legs 1 and 4 and legs 2 and 3 corresponded to $V_{\mathrm{L2}} = 0$ and $V_{\mathrm{R2}} = 0$. Under non-ideal load conditions, we aim to minimize the fundamental frequency component of V_{L2} and V_{R2}. This is achieved by shifting the phase slightly between legs 1 and 4 and also between legs 2 and 3 such that the fundamental frequency component of V_1, V_4 and V_2, V_3 each have the same phase, thus minimizing the voltage difference.

The gate signals for legs 1 and 4 after phase adjustment are shown in Fig. 6. Leg 1 is hard switching and leg 4



(a) Leg Voltage (b) Tx Coil Current

Fig. 5. Simulation results under ideal load conditions.

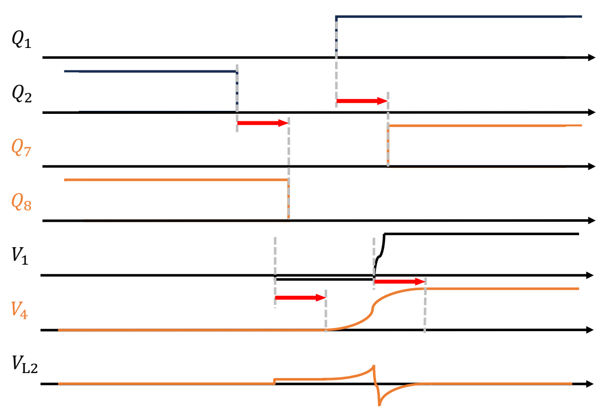


Fig. 6. Phase adjustment control

achieves ZVS, so the phase of leg 4 is slightly lagged, and the fundamental frequency component of V_{L2} is suppressed.

A. Numerical Analysis

For resonant DWPT systems, the resonant frequency is the dominant element of inactive coil current. For leg voltage V_n (n=1,2,3,4),

$$V_n = A_n e^{j\phi_n} \tag{1}$$

where A_n is the amplitude and ϕ_n is the phase of the resonant frequency component of each leg voltage. Variations in I_{L1} and I_{R1} result in variations of the leg voltage waveform during deadtime, and the resulting voltage can be expressed as follows.

$$V_n' = A_n' e^{j\phi_n'} \tag{2}$$

Therefore,

$$I_{\mathrm{L2}} = \frac{V_1' - V_4'}{Z_{\mathrm{L2}}} \tag{3}$$

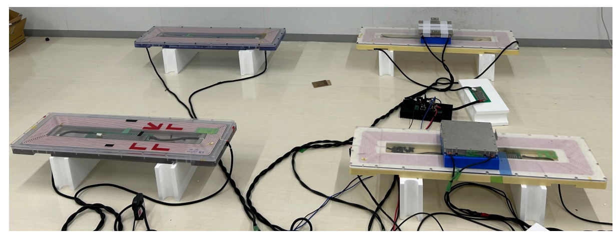


Fig. 7. The 4 Tx coils and 2 Rx coils used for the experiment.

where $Z_{\mathrm{L2}} = R_{\mathrm{L2}} + j\left(2\pi f L_{\mathrm{L2}} - \frac{1}{2\pi f C_{\mathrm{L2}}}\right)$.

$$|V_1' - V_4'| = A_1'^2 + A_4'^2 - 2A_1'A_4' \cos\left(\phi_1' - \phi_4'\right) \tag{4}$$

Assuming the inactive coil current is sufficiently small compared to the active coil current such that its effect on A_1' and A_4' are negligible, a phase difference of $\phi_1' - \phi_4'$ between the gate signals of legs 1 and 4 would minimize the inactive coil current. As the voltage variation is confined to the dead-time, the optimal phase difference for minimizing inactive coil current ϕ_{opt} should exist such that $-2\pi\frac{t_{\mathrm{dt}}}{T} \leq \phi_{\mathrm{opt}} \leq 2\pi\frac{t_{\mathrm{dt}}}{T}$, where t_{dt} is the length of deadtime and T is the period.

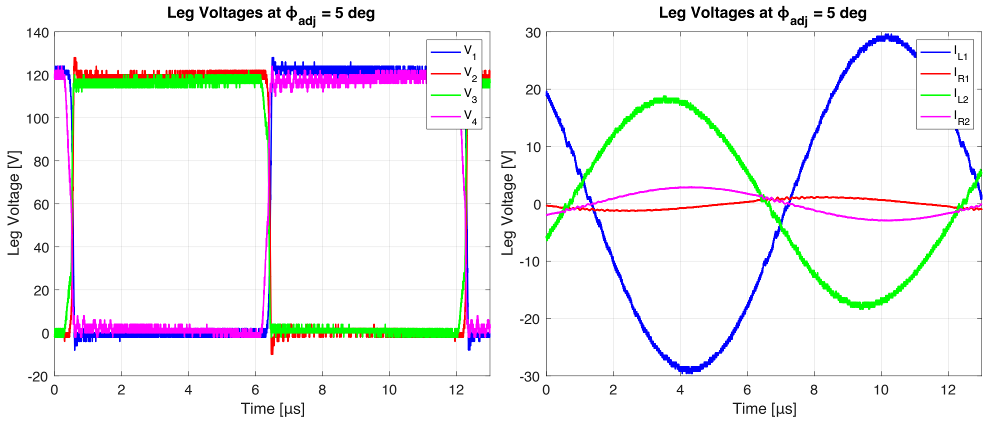
EXPERIMENTS

Setup

Experiments were conducted to verify the 4LL inverter. The circuit is shown in Fig. 2(b). Table I shows the parameters of the setup. The Tx and Rx coils used are shown in Fig. 7.

Experiment Results

Fig. 8 shows the leg voltage and Tx current waveforms after phase adjustment. Current through the inactive coils I_{L2} and I_{R2} are greatly reduced compared to I_{L1} and I_{R1}. Unlike in the ideal case, the inactive coil currents are not entirely suppressed. This is likely due to variations in the output capacitance of the MOSFETs used in the experiments. Experiments using MOSFETs with less parameter variations, which will be closer to actual DWPT conditions, are required.



(a) Leg Voltage (b) Tx Coil Current

Fig. 8. Experimental results after phase adjustment

TABLE I
CIRCUIT PARAMETERS.

Parameter	Symbol	Value
DC Voltage	V_{DC}	120 [V]
Battery Voltage	V_{Batt}	120 [V]
Tx resistance	R_{L1},R_{R1},R_{L2},R_{R2}	270, 150, 440, 300 [mΩ]
Tx inductance	L_{L1},L_{R1},L_{L2},L_{R2}	242, 238, 239, 242 [µH]
Tx capacitance	C_{L1},C_{R1},C_{L2},C_{R2}	14.5, 14.6, 14.6, 14.5 [nF]
Rx resistance	R_{Lr}, R_{Rr}	120, 110 [mΩ]
Rx inductance	L_{Lr}, L_{Rr}	150, 149 [µH]
Rx capacitance	C_{Lr}, C_{Rr}	23.4, 23.4 [nF]
Mutual inductance	M_{L}, M_{R}	20, 20 [µH]
Resonant frequency	f	85 [kHz]

The difference in transmitter current is due to variations in the compensation capacitance, and will be addressed in future experiments.

Fig. 9 shows the results of phase adjustment on the inactive coil currents. The results show the effectiveness of the proposed phase adjustment for reducing inactive coil current. Here, too, the ideal phase for minimum current doesn't match between I_{L2} and I_{R2} due to differences in output capacitance of the MOSFETs.

CONCLUSION

In this paper, a novel inverter topology called the 4-legged loop (4LL) inverter was proposed for 2-lane DWPT, and its operational principles were outlined. Phase adjustment control was proposed to account for uneven load, and its effectiveness was shown in simulations and experiments. For future works, simultaneous control of left and right circuits will be researched, as well as application to DWPT settings.

ACKNOWLEDGMENT

This paper is based on results obtained from a project, JPNP21028, subsidized by the New Energy and Industrial Technology Development Organization (NEDO).

This work was supported by JST SPRING, Grant Number JPMJSP2108.

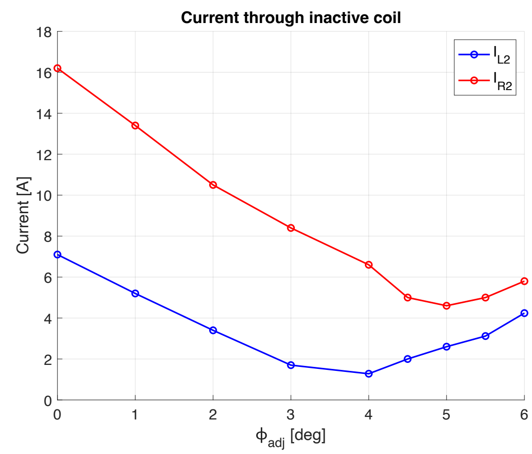


Fig. 9. Results of phase adjustment

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