Resonant Capacitor Voltage Based 85-kHz 3-kW Synchronous Rectification on Wireless Power Transfer System

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Abstract-A wireless power transfer (WPT) system has been considered to be applied to various charging applications. Conversion efficiency is one of the important factors and is in need of improvement in various approaches. This paper proposes a WPT system consisted of a synchronous rectification without transfer side signals. The proposed rectifier is applied to a magneticfield WPT system with a series-series topology. This system is characterized by the use of the voltage sensor at the secondary resonant capacitor to achieve the synchronous rectification. The theoretical analysis concludes by the secondary resonant capacitor voltage being 90 degrees forward from the rectifier input voltage. A synchronous rectifier is designed, constructed, and tested to verify the principles of operation. The conversion efficiency of the proposed synchronous system from dc to dc is 91.8% achieved at 85-kHz 3-kW output power and 1.6pt higher than the diode rectifier method. The efficiency distribution results from the loss of the synchronous rectifier is 53.2 W lower than that of the diode rectifier.

Index Terms—Inductive power transfer, magnetic-field wireless power transfer, synchronous rectification, wireless power transfer, voltage sensor

I. INTRODUCTION

Wireless power transfer (WPT) system has been widely considered as a charging application in terms of research and development [1]- [7]. The system is expected to be applied to drones [3], automatic underwater vehicles [4], and electric vehicles (EVs) [5]- [7] since the WPT system has no electrical contact, thus bringing safety, convenience, and easiness for users. The WPT systems for EVs are considered to be separately produced as primary (transfer-side) assemblies and secondary (receiving-side) assemblies by each manufacturer respectively. In order to spread WPT systems for EVs and

improve usability, the possibility of power transfer is needed to guarantee even different manufacturers' combinations. Thus, some standardizing organizations are now discussed about international standards in WPT system for EVs, especially magnetic-field WPT system (inductive power transfer) [8]-[10]. SAE J2954 working group [8] defines some classifications which are included in the transfer air gap, interoperable level, and power transfer. For example, the classification of power transfer levels is separated into 3 classes which are defined by the input power from the grid and are regulated by 3.7 kVA, 7.7 kVA, and 11.1 kVA. Also, they regulate various performances in order to keep interoperability between primary and secondary side assemblies or safety for users. One of these regulated performances, conversion efficiency from the grid to a battery needs to be over 85% at nominal alignment which is the point of maximum efficiency. Also, efficiency being over 80% at offset position means misalignment condition [10].

A magnetic-field WPT system consists of 4 components. The first component is a grid to dc converter. The second is an inverter to achieve dc to high-frequency ac. The third is WPT parts which transfer power using a magnetic field. The last component is a rectifier to convert from high-frequency ac to dc. In order to increase conversion efficiency, it needs to decrease the loss of each component in the WPT system. In the rectifier, the power loss caused by the forward voltage drop of diodes is large at high current conditions. To cope with the diode voltage, some papers have reported the synchronous rectification of WPT systems: One leg of a rectifier has consisted of FETs, and the other has been diodes [11]. One timing controller of the synchronous rectifier is generated by communication with the ground side [12]. The other controller is made by secondary current [13], [14]. Using a rectifier controller, the system has a wide operating range regarding

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Fig. 1. Concept of the proposed wireless power transfer system.

coupling factor, battery voltage variation, and partial load [15]. The WPT system with pulse width control at receiving side using a resonant capacitor voltage performs 400 W power transfer configured with a DSP and an analog PLL circuit [16].

The receiving-side assembly is not easy to get a synchronous signal for the rectification in a WPT system from the transfer-side assembly at market products. Since the WPT system is made separately on the transfer-side and the receivingside assemblies which are not electrically connected. Therefore, if the transfer-side assembly tries to send a synchronous signal to the receiving side, advanced communication devices are required in each assembly. To simplify the synchronous WPT system, it needs to detect the synchronous signal independently on the receiving side.

This paper proposes a full-digital control method for the synchronous rectifier on the WPT system. The series-series topology WPT system is selected to achieve the proposed method. The synchronous signal for the rectifier uses a voltage sensor of the secondary resonant capacitor voltage. This method is a simple configuration and minimizes the cost to achieve synchronous rectification, not using advanced communication with the transfer side and a high-frequency highcurrent sensor on the secondary side. Theoretical analysis of an equivalent transformer model is done at WPT parts on how to detect the synchronous signal and demonstrates basic theories. The WPT system, which adopted the synchronous rectifier is constructed and tested to verify fundamental characteristics including waveforms, transfer power, and components' efficiencies.

II. THEORETICAL ANALYSIS AND CONTROL METHOD

A. Main Circuit Configuration

Fig. 1 shows the circuit configuration of a WPT system in this experiment, which is based on the so-called "seriesseries" WPT system [17]. A full-bridge inverter operating at a high frequency of 85 kHz is used for the proposed WPT system. The switching devices used in the inverter are SiC MOSFETs. The primary coil and the secondary coil are connected in series with the primary resonant capacitor $C_{\rm P}$ and the secondary resonant capacitor $C_{\rm S}$, respectively. A singlephase full-bridge synchronous rectifier is used to achieve acto-dc power conversion at the receiving end. The devices are also used for SiC MOSFETs. A load is a constant voltage load instead of a battery. The positive directions of each voltage and current are defined, respectively, as shown in Fig. 1.



Fig. 2. Equivalent circuit to the SS topology WPT system.

B. WPT Circuit Analysis

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Fig. 2 shows an equivalent circuit of the WPT system at a fundamental frequency of 85 kHz in Fig. 1. The winding resistances take account of skin effect and proximity effect and the equivalent ferrite-core-loss resistance. At first, these resistances are eliminated from the following analysis. The input voltage and angular frequency are represented as $V_{\rm IN}$ and ω , assuming a sinusoidal voltage. The self inductances of the primary coil and the secondary coil are defined as $L_{\rm P}$ and $L_{\rm S}$, respectively. The mutual inductance between the primary and secondary coils is defined as M. The current and voltage directions are defined as shown in Fig. 2. The back electromotive forces $V_{\rm P}$ and $V_{\rm S}$ are given by a function of the primary and secondary coil currents $I_{\rm IN}$ and $I_{\rm O}$ as follows:

$$V_{\rm P} = j\omega L_{\rm P} I_{\rm IN} + j\omega M I_{\rm O}.$$
 (1)

$$V_{\rm S} = j\omega M I_{\rm IN} + j\omega L_{\rm S} I_{\rm O}.$$
 (2)

Two resonant capacitors are determined from ((3)) [17].

$$\omega = \frac{1}{\sqrt{C_{\rm P}L_{\rm P}}} = \frac{1}{\sqrt{C_{\rm S}L_{\rm S}}} \tag{3}$$

These resistances $r_{\rm P}$ and $r_{\rm S}$ which are much lower than the mutual and self reactances at the resonant frequency are eliminated from the following analysis, and further analysis was made in [18]. The input and output voltage are calculated as

$$V_{\rm IN} = j\omega M I_{\rm O}.$$
 (4)

$$V_{\rm O} = j\omega M I_{\rm IN}.$$
 (5)

Eq. (4) indecate the output current $I_{\rm O}$ is proportional to input voltage $V_{\rm IN}$.

C. Synchronized Control Circuit Configuration

Discussing above, the power factors at output voltage $V_{\rm O}$ and current $I_{\rm O}$ in Fig. 2 should be unity for maximize active power transfer.

$$V_{\rm O} = -R_{\rm O}I_{\rm O}.\tag{6}$$

From (6), the synchronous rectification is established by detecting the polarity of the current. In the SS topology WPT system described in fig. 1, the output current $I_{\rm O}$ is almost a sinusoidal wave since the circuit is resonant conditions shown in (3). The secondary resonant capacitor voltage $V_{\rm CS}$ gives

$$V_{\rm CS} = -\frac{I_{\rm O}}{j\omega C_{\rm S}}.\tag{7}$$



Fig. 3. The block diagram for the proposed synchronous rectification of the SS topology WPT system.



Fig. 4. Photograph of the mounted secondary resonant capacitor board in this paper.

Substituting (6) into (7) as

$$V_{\rm O} = -j \frac{R_{\rm O}}{\omega C_{\rm S}} V_{\rm CS}.$$
 (8)

Eq. (8) shows that $V_{\rm CS}$ is 90 degrees forward by $V_{\rm O}$. The synchronous rectification is formed by detecting $V_{\rm CS}$ in the same way as the output current and delaying it by 90 degrees. Substituting eq. (4) into eq. (7) as

$$V_{\rm CS} = \frac{1}{\omega^2 C_{\rm S} M} V_{\rm IN}.$$
(9)

Eq. (9) shows that $V_{\rm CS}$ is the same phase of $V_{\rm IN}$ and does not depend on load resistance $R_{\rm O}$.

Fig. 3 shows the proposed diagram for the synchronous rectification. The diagram just needs the polarity of $V_{\rm CS}$. The resonant capacitor voltage of the SS topology WPT system is several kilo-volts as the power increases. Therefore, several capacitor chips are connected in series to form the resonant capacitor. The divided voltage is obtained from one chip of the resonant capacitors composed of multiple capacitor chips in series. The resonant capacitor voltage is further divided to be input to the comparator. The output signal $S_{\rm comp}$ of the comparator which waveform is square shape was isolated and input the digital signal to the FPGA. The gate signal $g_{\rm XP}$ is generated by the FPGA after calculating the delay time $t_{\rm delay}$.

Fig. 4 shows the mounted secondary resonant capacitor board in this paper. The board is shown on the right-side diagram of fig. 3. The upper terminal is connected to the synchronous rectifier, the other is connected to the secondary coil. The capacitor board is fabricated in eight series and twelve parallel capacitor chips. Besides, resistors are installed



Fig. 5. Photograph of the experimental converter board.

in parallel on the chips to suppress the imbalance of the chip voltage due to element variations which the value is 91 k Ω . In the actual capacitor, not only the pure capacitance component but also the effective series resistance and effective series inductance exists. At the fundamental frequency of this experiment, the angle of the capacitor impedance is 7.79×10^{-3} deg. which value is negligibly small.¹

When using a high-frequency, large-current current sensor for synchronous rectification, it is necessary to consider the delay of the current sensor. Comparing the output value of the current sensor CTL-12-S30-2.5Z produced by U.R.D. Co. Ltd. that can be mounted on the board with a current probe TCP0020 Tektronix, it was found that the sensor output was delayed by about 1.6 μ s compared to the current probe. Furthermore, it was found that even with the same current sensor, there is a difference of about 300 ns between the minimum and maximum delay values. The problem is that the specifications of the current sensor do not compensate for the delay. When using a current sensor with a large delay time error, it is necessary to calibrate the delay time for each device. Furthermore, due to the delay, it is difficult to generate gates within the same timing at each current sensor. On the other hand, when the detecting voltage method is used, it is composed of a passive component consisting of resistors, capacitors, and ICs, and it is easy to estimate and design the delay time of the proposed method. From the above, when a voltage sensor is used, an additional insulating element is required, but it can be configured without using an expensive current sensor, and the board area can be reduced.

III. EXPERIMENTAL RESULT

A. Experimental Setup

Fig. 5 shows the synchronous rectification converter board used in this paper. The SiC half-bridge modules are mounted on the backside of the converter board at the two capacitors where the blue squares are indicated in fig. 5. The yellow square part is the implementation of the synchronous rectification control circuit shown in fig. 3. The isolated synchronous signal is connected to the FPGA board through the connector on the lower right. The voltage, current, and temperature of

¹The capacitors used in this experiment are CKG32KC0G3A223J335AJ made by TDK.



Fig. 6. Photograph of the experimental wireless power transfer system.



Fig. 7. Experimental results of the WPT system with diode rectification shown in fig. 1 at $V_{\rm DC}$ = 190 V, $V_{\rm L}$ = 280 V. (a) Waveforms of inverter output voltage $v_{\rm IN}$ and current $i_{\rm IN}$. (b) Waveforms of rectifier input voltage $v_{\rm O}$ and current $i_{\rm O}$.

the SiC devices are also monitored by the FPGA for safety through the two connectors. The phase locking loop (PLL) and the delay algorithms are shown in fig. 3 programmed on the FPGA board as an MWPE4-FPGA6.

Fig. 6 shows the photograph of the synchronous WPT system used in the following experiments. PE-Expert4 is installed on the upper right side of the photo, and the synchronous rectification board is installed under the board. The secondary resonant capacitor is placed on the right side of the board, and



Fig. 8. Experimental graphs of the synchronous WPT system shown in fig. 1 at $V_{\rm DC}$ = 190 V, $V_{\rm L}$ = 280 V. (a) Waveforms of inverter output voltage $v_{\rm IN}$ and current $i_{\rm IN}$. (b) Waveforms of synchronous rectifier input voltage $v_{\rm O}$ and current $i_{\rm O}$. (c) Waveforms of upper gate signal at synchronous rectifier $g_{\rm XP}$ and lower signal $g_{\rm XN}$. (d) Waveforms of the secondary resonant capacitor volgate $v_{\rm CS}$ and the input signal of FPGA.



Fig. 9. Experimental Results the synchronous rectifier.

one capacitor chip is connected to the synchronous rectifier board displayed in fig. 3. The WPT coils are installed in the lower right. The inverter is installed in the gray box in the center. The input side ac/dc converter and the output side bidirectional ac/dc converter are arranged on the right side.

Table I shows the experimental transformer parameters of the WPT coils at 85 kHz defined by fig. 2 and measured by Hioki IM3533. The coupling coefficient is 0.157 in this paper. The primary resonant frequency defined at eq. (3) is 85.4 kHz, and the secondary frequency is 86.1 kHz. $\eta_{\rm max}$ and $R_{\rm Omax}$ are 98.73% and 7.63 Ω , respectively.

B. Experimental Result of Power Transfer

Fig. 7 shows the experimental waveforms of $v_{\rm IN}$, $i_{\rm IN}$, $v_{\rm O}$, and $i_{\rm O}$, under the diode rectifier operation in fig. 1 at $P_{\rm L}$ = 3 kW for adjusting input dc voltage. Other parameters are shown in table I and the input dc voltage $V_{\rm DC}$ and output dc voltage $V_{\rm L}$ are 190 V and 280 V, respectively. The output dc voltage is determined by the lower limit of the battery voltage of SAE J2954 for the large output current condition [8]. The operating frequency of the inverter is 85.5 kHz. The currents $i_{\rm IN}$ and $i_{\rm O}$ are 19.6 Arms and 12.0 Arms in this condition, respectively. The input current $i_{\rm IN}$ is delayed by 0.60 $\mu {\rm sec}$ from the input voltage $v_{\rm IN}$ according to protect the ground-side inverter in fig. 7 (a). Besides, the output current $i_{\rm O}$ is also delayed by 90 degrees from the input voltage $v_{\rm IN}$ derived eq. (4). The output current $i_{\rm O}$ is inverted by 180 degrees from the output voltage $v_{\rm O}$ defined in fig. 1. The voltage fluctuation of $v_{\rm IN}$ which is near the zero-cross point of $i_{\rm IN}$ is due to the insufficient capacity of the input DC capacitor at the inverter.

Fig. 8 shows the experimental waveforms of v_{IN} , i_{IN} , v_O , i_O , g_{XP} , and g_{XN} under the voltage-detection synchronous



Fig. 10. Loss break down of WPT system at $P_{\rm L}$ = 3 kW. The top values of the bars are conversion efficiency in the below components.

rectifier operation in fig. 1 at $P_{\rm L}$ = 3 kW. The $g_{\rm XP}$ and $g_{\rm XN}$ are gate voltage of SiC devices defined by fig. 1. The experimental parameters are the same in fig. 7 without the synchronous rectifier operation. Other parameters are shown in table I and the input dc voltage $V_{\rm DC}$ and output dc voltage $V_{\rm L}$ are 190 V and 280 V, respectively. The output dc voltage is determined by the lower limit of the battery voltage of SAE J2954 for the large output current condition [8]. The operating frequency of the inverter is 85.5 kHz. The delay time t_{delay} of the gate signals shown in fig. 3 is controlled to be the same output power at the diode condition. These currents are 19.3 Arms and 12.0 Arms in this condition, respectively. The input current $i_{\rm IN}$ is delayed by 0.64 μ sec from the input voltage $v_{\rm IN}$ according to protect the ground-side inverter in fig. 8 (a). Besides, the output current $i_{\rm O}$ is also delayed by 90 degrees from the input voltage $v_{\rm IN}$ derived eq. (4). The output current $i_{\rm O}$ is inverted by 180 degrees from the output voltage $v_{\rm O}$ defined in fig. 1. The gate signals between $g_{\rm XP}$ and $g_{\rm XN}$ are designed 800 ns dead time not to short circuit in the converter leg. The secondary resonant capacitor voltage $v_{\rm Sc}$ is ahead of 92.5 deg. from $i_{\rm O}$ derived in eq. (7). The rising voltage of the input signal of the FPGA $S_{\rm comp}$ is delayed by 760 ns, and the falling edge is 600 ns from $v_{\rm CS}$. This difference is caused that the propagation delay of the rising and falling voltage of the photocoupler (ACPL-M46T) used for isolation is different.

Fig. 9 shows experimental characteristics of the synchronous rectification which $V_{\rm DC}$ in Fig. 1 was adjusted from 110 to 190 V. The conversion efficiency η from input dc source to output dc load was measured as 91.8% and 90.2% at $V_{\rm DC} = 190$ V, $V_{\rm L} = 280$ V, and $P_{\rm L} = 3.0$ kW with the synchronous control and the diode rectification, respectively. The output voltage in this changing input voltage experiment is the same as these ones. As shown in eq. (4), the output voltage is constant, so the output power is in the liner to the input voltage.

Fig. 10 and Table II show the loss break downs of the diode and synchronous rectifier WPT system at $P_{\rm L} = 3$ kW and the conversion efficiencies in each component. The

TABLE II EXPERIMENTAL CONVERSION EFFICIENCY OF EACH COMPONENT AT $P_{1}=3 \text{ kW}$

	Inverter	WPT coil	Rectifier	dc to dc
Diode	98.7%	97.4%	93.7%	90.2%
Synchronous	98.6%	97.7%	95.3%	91.8%

efficiency of the inverter component is almost the same in the two rectifications. For the WPT coil component, the loss of the synchronous rectification was slightly lower by 9.07 W. Since the output resistance of the synchronous mode is close to the optimum resistance R_{Omax} = 7.8 Ω which value of synchronous rectification is 22.2 Ω and diode rectification is 22.6 Ω . As shown in Table I, the optimum efficiency of the WPT coil is 98.73%, but the experimental results are about 1 point lower. There are because the output impedance is higher than the optimum load resistance and does not completely satisfy the resonance conditions shown in the eq. (3). Regarding the rectifier section, the loss of about 53.2 W is lower when synchronous rectification is performed than when diode rectification is performed. It is considered that this is because not only the conduction loss due to the forward voltage drop of the diode is reduced, but also the switching loss is reduced.

IV. CONCLUSION

This paper has proposed a novel control method for a synchronous rectifier at a 3-kW 85-kHz wireless power transfer system. The gate signals of the synchronous rectifier have been generated by the secondary-side resonant capacitor voltage and constructed full-digital processing with FPGA. The method decreases the cost not to use advanced communications with the ground side or a high frequency current sensor and is easy to design the delay time of the control circuit compared to a current sensor method. Theoretical analysis of a series-series WPT system concludes that the voltage detection method was worked instead of the output current detection method. The WPT system installed in the synchronous rectifier has been designed, constructed, and tested to verify the proposed method. The dc to dc conversion efficiencies have been compared between synchronous and diode rectifiers. The synchronous rectifier has improved the efficiency by 1.6 points compared to the diode one at 3 kW output load. The efficiency distribution has resulted in the loss of the synchronous rectifier which was 53.2 W lower than that of the diode rectifier. It has been verified that the secondary voltage sensor based synchronous rectification improves the conversion efficiency.

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